WHAT IS CLAIMED IS:

1. An image display apparatus for multiple tone display with number of gradation levels determined by number of bits of an image signal of m bit digital data, comprising:

a display having data holding function for holding data in pixels arranged on a matrix and performing display according to held data;

a vertical drive circuit sequentially and selectively scanning matrix form display elements forming said display per row;

a horizontal drive circuit writing a voltage among binary voltage preliminarily assigned depending upon the digital data of the image signal to be displayed in the display elements in the row selected by the vertical drive circuit,

said horizontal drive circuit and said vertical drive circuit being operated for performing selective scan of respective display element for at least m times in one frame period in synchronism with said image signal to be displayed, and

said vertical drive circuit being constituted of n in number of sequence circuits and logic operation circuits for outputs of said sequence circuits, which n is smaller than m, a period from inputting to said sequence circuit to outputting from the final stage being less than or equal to half of one frame period, and at least one of said sequence circuits being used

with selectively inputting a plurality of inputs.

2. An image display apparatus for multiple tone display with number of gradation levels determined by number of bits of an image signal of m bit digital data, comprising:

a display having data holding function for holding data in pixels arranged on a matrix and performing display according to held data;

a vertical drive circuit sequentially and selectively scanning matrix form display elements forming said display per row;

a horizontal drive circuit writing a voltage among binary voltage preliminarily assigned depending upon the digital data of the image signal to be displayed in the display elements in the row selected by the vertical drive circuit,

said horizontal drive circuit and said vertical drive circuit being operated for performing selective scan of respective display element for at least m times in one frame period in synchronism with said image signal to be displayed, and display period being preliminarily determined depending upon the digital data of the image signal to be displayed, and

said vertical drive circuit being constituted of n in number of sequence circuits and logic operation circuits for outputs of said sequence circuits, which n is smaller than m, a period from inputting to said sequence circuit to outputting from the final stage

being shorter than a minimum value of sums of arbitrarily selected sequentially input n bit display periods, and at least one of said sequence circuits being used with selectively inputting a plurality of inputs.

3. An image display apparatus as set forth in claim 2, wherein when a luminous period of the maximum weighted bit is longer than said period from inputting to said sequence circuit to outputting from the final stage, said luminous period is divided into half to be dividedly input by twice inputs on one frame period.

4. An image display apparatus as set forth in claim 1, wherein said vertical drive circuit generates a scanning pulse not corresponded to the digital data of said image signal and, for the row selectively scanned by said scanning pulse, all data from said horizontal drive circuit are held not displayed.

5. An image display apparatus for multiple tone display with number of gradation levels determined by number of bits of an image signal of m bit digital data, comprising:

a display having data holding function for holding data in pixels arranged on a matrix and performing display according to held data;

a vertical drive circuit sequentially and selectively scanning matrix form display elements forming said display per row;

a horizontal drive circuit writing a voltage

among binary voltage preliminarily assigned depending upon the digital data of the image signal to be displayed in the display elements in the row selected by the vertical drive circuit,

said horizontal drive circuit and said vertical drive circuit being operated for performing selective scan of respective display element for at least m times in one frame period in synchronism with said image signal to be displayed, and

in synchronism with the row selectively scanned by said vertical drive circuit, said horizontal drive circuit being constituted of n in number of line data latch circuits, which n is smaller than m, a display signal for said display elements being output depending upon logical signals each contains a product of an output of the line data latch circuit per bit and a control signal dividing the horizontal scanning period, and at least one of said line data latch circuit being used with selectively inputting a plurality of inputs.

6. An image display apparatus as set forth in claim 1, wherein said vertical drive circuit determines a voltage to be applied to a vertical scanning line of said active matrix depending upon a result of sequentially summing of logical signals containing products of multiplication of result of logical operation of the outputs of said sequence circuits and control signals dividing the horizontal scanning period.

7. An image display apparatus as set forth in claim 5, wherein said display element includes a first thin film transistor connected to the vertical scanning line of said active matrix at gate and to horizontal scanning lines at drain, source of said first thin film transistor is connected to a gate of a second think film transistor and an electrode of a storage capacitor, and an organic LED is connected to said second think film transistor so that a current continuously flow through said organic LED during a period in which the image signal is held in said storage capacitor.

8. An image display apparatus as set forth in claim 5, wherein said vertical drive circuit and said horizontal drive circuit are formed with thin film transistors on an active matrix substrate.

9. An image display apparatus forming a display and a drive circuit on a substrate for performing multiple tone display with number of gradation levels determined by number of bits of an image signal of m bit digital data, comprising:

said drive circuit including a vertical drive circuit and a horizontal drive circuit, said vertical drive circuit being constituted of n in number of sequence circuits and logic operation circuits for outputs of said sequence circuits, which n is smaller than m, and at least one of said sequence circuits being used with selectively inputting a plurality of

inputs.

10. An image display apparatus forming a display and a drive circuit on a substrate for performing multiple tone display with number of gradation levels determined by number of bits of an image signal of m bit digital data, comprising:

said drive circuit including a vertical drive circuit and a horizontal drive circuit, said horizontal drive circuit being constituted of n in number of line data latch circuits and logic operation circuits for outputs of said sequence circuits, which n is smaller than m, and at least one of said line data latch circuits being input a plurality of bit data, said display being controlled depending upon a result by sequentially summing logical signals containing products of multiplication of output of the line data latch circuit per bit and the control signal dividing the horizontal scanning period.

11. An image display apparatus as set forth in claim 10, which performs multiple tone display of the image signal of 6-bit digital data by controlling display period weighted depending upon each bit in one frame,

said vertical drive circuit includes three sequence circuits and logic operation circuits respectively connected to output ends of said sequence circuits, performs selective scan for respective display pixels for at least seven times in one frame

with dividing luminous period of the bit at which the weight is maximum, and order of input of the bit data being determined so that a minimum value of sums of arbitrarily selected sequent three luminous period becomes greater than a period from inputting to said sequence circuit to outputting from the final stage.

12. An image display apparatus as set forth in claim 10, which performs multiple tone display of the image signal of 8-bit digital data by controlling display period weighted depending upon each bit in one frame,

said vertical drive circuit includes three sequence circuits and logic operation circuits respectively connected to output ends of said sequence circuits, performs selective scan for respective display pixels for at least nine times in one frame with dividing luminous period of the bit at which the weight is maximum, and order of input of the bit data being determined so that a minimum value of sums of arbitrarily selected sequent three luminous period becomes greater than a period from inputting to said sequence circuit to outputting from the final stage.

13. An image display apparatus for multiple tone display of an image signal of digital data;

a memory for storing at least one frame of digital image signal input;

a display having data holding function in pixels arranged on matrix, for displaying according to

held data;

a vertical drive circuit for sequentially and selectively scanning matrix form display elements forming said display per row;

a horizontal drive circuit for writing a voltage among binary voltage preliminarily assigned depending upon the digital data of the image signal to be displayed in the display elements in the row selected by the vertical drive circuit,

a pulse generation circuit for generating a scanning pulse for driving respective of said horizontal drive circuit and said vertical drive circuit;

a bit selection circuit for selectively switching said vertical scanning pulse and the image data output upon inputting to respective of said vertical drive circuit and said horizontal drive circuit; and

a control circuit for controlling each scanning pulse and the output of said memory for synchronization at said display element.

14. An image display apparatus as set forth in claim 13, wherein said display, said vertical drive circuit and said horizontal drive circuit are formed on the same substrate.

15. An image display apparatus for multiple tone display of an image signal of digital data;

a memory for storing at least one frame of digital image signal input;

a display having data holding function in pixels arranged on matrix, for displaying according to held data;

a vertical drive circuit for sequentially and selectively scanning matrix form display elements forming said display per row;

a horizontal drive circuit for writing a voltage among binary voltage preliminarily assigned depending upon the digital data of the image signal to be displayed in the display elements in the row selected by the vertical drive circuit,

a pulse generation circuit for generating a scanning pulse for driving respective of said horizontal drive circuit and said vertical drive circuit;

a bit selection circuit for selectively switching said vertical scanning pulse and the image data output upon inputting to respective of said vertical drive circuit and said horizontal drive circuit; and

a control circuit provided on the same substrate with said vertical drive circuit and said horizontal drive circuit, for controlling each scanning pulse and the output of said memory for synchronization at said display element.